



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of

NEVILL, E.

Atty. Ref.: 550-513

Serial No. 10/781,867

TC/A.U.:

Filed: February 20, 2004

Examiner:

For: MEMORY RECYCLING IN COMPUTER SYSTEMS

\* \* \* \* \*

March 31, 2004

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

**INFORMATION DISCLOSURE STATEMENT**

As suggested by 37 C.F.R. 1.97, the undersigned attorney brings to the attention of the Patent and Trademark Office the references listed on the attached form PTO-1449, a copy of each non-U.S. patent being enclosed. This is not to be construed as a representation that a search has been made or that no better prior art exists, or that a reference is relevant merely because cited.

The Examiner is requested to initial the attached form PTO-1449 and to return a copy of the initialed document to the undersigned as an indication that the attached references have been considered and made of record.

Respectfully submitted,

**NIXON & VANDERHYTE P.C.**

By: 

Stanley C. Spooner  
Reg. No. 27,393

SCS:ecb

1100 North Glebe Road, 8th Floor

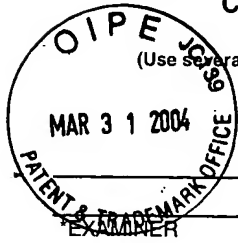
Arlington, VA 22201-4714

Telephone: (703) 816-4000

Facsimile: (703) 816-4100

INFORMATION DISCLOSURE  
CITATION

(Use several sheets if necessary)



Atty. Docket No.

Serial No.

550-513

10/781,867

Applicant

NEVILL, E.

Filing Date

Group

February 20, 2004

## U.S. PATENT DOCUMENTS

INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	3,889,243	6/1975				
	4,236,204	11/1980				
	4,587,632	5/1986				
	4,969,091	11/1990				
	4,922,414	5/1990				
	5,136,696	8/1992				
	5,455,775	10/1995				
	5,619,665	4/1997				
	5,638,525	6/1997				
	5,659,703	8/1997				
	5,740,461	4/1998				
	5,742,802	4/1998				
	5,752,035	5/1998				
	5,784,584	7/1998				
	5,809,336	9/1998				
	5,838,948	11/1998				
	5,875,336	2/1999				
	5,892,966	4/1999				
	5,925,123	7/1999				
	5,926,832	7/1999				
	5,937,193	8/1999				
	5,953,741	9/1999				
	6,003,126	12/1999				
	6,009,499	12/1999				
	6,009,509	12/1999				
	6,014,723	1/2000				
	6,021,469	2/2000				
	6,026,485	2/2000				
	6,031,992	2/2000				
	6,038,643	3/2000				
	6,070,173	5/2000				
	6,088,786	7/2000				
	6,122,638	9/2000				
	6,125,439	9/2000				
	6,148,391	11/2000				
	6,298,434	10/2001				
	6,317,872	11/2001				
	6,338,134	1/2002				
	6,349,377	2/2002				
	6,374,286	4/2002				
	6,606,743	8/2003				

\*Examiner

Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application.

INFORMATION DISCLOSURE  
CITATION

(Use several sheets if necessary)

Atty. Docket No.

Serial No.

550-513

10/781,867

Applicant

NEVILL, E.

Filing Date

Group

February 20, 2004

## FOREIGN PATENT DOCUMENTS

					TRANSLATION			
DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	YES	NO		

## OTHER DOCUMENTS (including Author, Title, Date, Pertinent pages, etc.)

	H. Stone, Chapter 12 - "A Pipeline Push-Down Stack Computer", 1969, pages 235-249
	C. Glossner et al, "Delft-Java Link Translation Buffer", 8/1998.
	N. Vijaykrishnan et al, "Object-Oriented Architectural Support For a Java Processor" 1998, pages 330-355
	C. Glossner et al, "The Delft-Java Engine: An Introduction", 8/1997
	K. Ebcioglu et al, "A Java ILP Machine Based On Fast Dynamic Compilation", 1/1997, pages 1-13
	A. Wolfe, "First Java-specific chip takes wing" <i>EETimes</i> - 1997
	Y. Patt, <i>Introduction to Computing Systems From Bits and Gates to C and Beyond</i> , 1999, pages 1-517
	M. Ertl, "Stack Caching for Interpreters" 1994, pages 1-10
	M. Ertl, "Stack Caching for Interpreters" 1995, pages 1-13
	M. Ertl, "Implementation of Stack-Based Languages on Register Machines" 4/1996, pages 1-4
	K. Andrews et al, "Migrating a CISC Computer Family Onto RISC Via Object Code Translation" 1992, pages 213-222
12	J. O'Connor et al, "PicoJava I Microprocessor Core Architecture" 10/1996, pages 1-8, Sun Microsystems
	M. Ertl, "A New Approach to Forth Native Code Generation" 1992
	M. Maierhofer et al, "Optimizing Stack Code" 1997, page 1-9
	D. Ungar et al, "Architecture of SOAR: Smalltalk on a RISC" The 11 <sup>th</sup> Annual International Symposium on Computer Architecture, 6/1984, pages 188-197
	O. Steinbusch, "Designing Hardware to Interpret Virtual Machine Instructions" 2/1998, pages 1-59
	R. Kapoor et al, "Stack Renaming of the Java Virtual Machine" 12/1996, pages 1-17
	A. Yonezawa et al, "Implementing Concurrent Object-Oriented Languages in Multicomputers" <i>Parallel and Distributed Technology (Systems and Applications)</i> 5/1993, pages 49-61
	C. Hsueh et al, "Java Bytecode to Native Code Translation; The Caffeine Prototype and Preliminary Results" IEEE/ACM International Symposium on Microarchitecture, 12/1996, pages 90-97
	Y. Patt et al, <i>Introduction to Computing Systems From Bits and Gates to C and Beyond</i> , 2001, pages 1-526
	Sun Microsystems PicoJava Processor Core Data Sheet, 12/1997, pages 1-11
	H. McGhan et al, PicoJava A Direct Execution Engine for Java Bytecode, 10/1998, pages 22-26
	C. Glossner et al, "Parallel Processing" Euro-Par 1997: Passau, Germany, 8/1997
	Y. Patt, <i>Introduction to Computing Systems From Bits and Gates to C and Beyond</i> , 1999, pages 10-12 & 79-82
	Espresso - The High Performance Java Core Specification, 10/2001, pages 1-33, Aurora VLSI, Inc.
	J. Gosling, "Java Intermediate Bytecodes" 1995, pages 111-118
	P. Koopman, Jr. "Stack Computers The New Wave" 1989, pages 1-234
	J. O'Connor et al, "PicoJava-I: The Java Virtual Machine in Hardware" <i>IEEE Micro</i> A Case for Intelligent RAM, March/April 1997, pages 45-53
	M. Mrva et al, "A Scalable Architecture for Multi-Threaded JAVA Applications" Design Automation and Test in Europe, 2/1998, pages 868-874
	L. Chang et al, "Stack Operations Folding in Java Processors" <i>IEEE Proc. - Comput. Digit. Tech.</i> , Vol. 145, No. 5, pages 333-340 9/1998
	L. Ton et al, Proceedings of the '97 International Conference on Parallel and Distributed Systems, "Instruction Folding in Java Processor", pages 138-143, 12/1997

\*Examiner

Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application.

INFORMATION DISCLOSURE  
CITATION

(Use several sheets if necessary)

Atty. Docket No.

Serial No.

550-513

10/781,867

Applicant

NEVILL, E.

Filing Date

Group

February 20, 2004

	K. Buchenrieder et al, "Scalable Processor Architecture for Java With Explicit Thread Support" <i>Electronics Letters</i> Vol. 33, No. 18, pages 1532+, 8/1997
	C. Chung et al, Proceedings of the '98 International Conference on Parallel and Distributed Systems, "A Dual Threaded Java Processor for Java Multithreading" pages 693-700, 12/1998
	I. Kazi et al, "Techniques for Obtaining High Performance in Java Programs" 9/2000, pages 213-240
	R. Kieburtz, "A RISC Architecture for Symbolic Computation" 1987, pages 146-155
	M. Berekovic et al, "Hardware Realization of a Java Virtual Machine for High Performance Multimedia Applications", pages 479-488, 1997
	M. Ibrahim et al.; "Signal Processing Systems (SIPS 97) Design and Implementation"; 1997 IEEE Workshop, 11/1997.
	P. Deutsch, "Efficient Implementation of the Smalltalk-80 System" 1983, pages 297-302
	J. Davis; "Rockwell Produces Java Chip" 9/1997, CNET NEWS.COM, pages 1 of 3.
	Y. Patt et al, <i>Introduction to Computing Systems from Bits and Gates to C and Beyond</i> , 2001, pages 1-16, 91-118 & 195-209

\*Examiner

Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application.